240IEE33 - Digital Electronic Systems

Coordinating unit: 240 - ETSEIB - Barcelona School of Industrial Engineering
Teaching unit: 710 - EEL - Department of Electronic Engineering
Academic year: 2017
Degree: MASTER'S DEGREE IN INDUSTRIAL ENGINEERING (Syllabus 2014). (Teaching unit Optional)
ECTS credits: 4.5
Teaching languages: Catalan

Teaching staff
Coordinator: EMILIO JOSE LUPON ROSES
Others: Lupon Roses, Emilio Jose

Opening hours
Timetable: Tuesday and Friday from 12 PM to 2 PM.

Degree competences to which the subject contributes

Specific:
CEELECT1. Design electronic systems (mixed analogical and digital systems and micro-mechanical systems on silicon, digital systems based on discrete components, logical programable devices and/or microprocessors, electronic instrumentation systems and power electronic systems) and manage development projects and/or commercialization of electronic systems or development projects and/or commercialization of systems in which the electronic subsystems have an important specific weight.
CEELECT3. Empower for the management of a product (product manager), technical management or innovative management of electronic products or which include electronic subsystems with an important specific weight.
CEELECT2. Analyse, diagnose and maintain the electronic systems and manage the maintenance equipment of electronic systems or of systems in which the electronic subsystems have an important specific weight.
Teaching methodology

This course has an assigned load of 4.5 ECTS credits, which is equivalent to 112.5 student's working hours. 44 of these hours correspond to face-to-face activities (28.5 hours of theory and problem lectures, 12 hours of laboratory experiments, of which 0.5 hours devoted to project definition, and 3.5 hours of assessments). The remaining 68.5 hours correspond to non-classroom activities (14.5 hours to complete the laboratory experiments, 25.5 hours to carry out the project, and 28.5 hours to study the theory).

The course is structured in two parts: a theory part and a laboratory part. Each one of these parts involves face-to-face activities, non-attending activities, and assessment activities.

Face-to-face activities of the theory part include 28.5 hours of lectures, where the above indicated content will be followed. These lectures will consist in theory lectures and problems and examples resolution and/or discussion, going from one activity to another at the discretion of the professor. The 28.5 hours of lectures are equivalent to 19 sessions of 1.5 hours. If the academic calendar does not allow these 19 sessions, some of them will last until 2 hours to make the total amount of 28.5 hours scheduled. Non-attending activities of the theory part consist in the study of the matter.

The laboratory part consists, on one hand, in carrying out a set of laboratory experiments and, on the other hand, in carrying out a project. Face-to-face activities of the laboratory part consist in 6 laboratory sessions of 2 hours, which will be held at the Laboratory of Electronics III, located on the 9th floor, door 45. In these sessions, the above indicated content will be followed, serving part of the first session for defining the project. Non-attending activities of the laboratory part, which are estimated in 40 hours, include finishing the laboratory experiments and carrying out the project. The practical part will be made individually.

Learning objectives of the subject

Understand the different characteristics and benefits of programmable logic devices in order to use them properly in the implementation of digital systems.

Knowing how to apply the design methodology of digital systems using different CAD tools, especially those based on the VHDL hardware description language.

Enable students to optimize the implementation of logic functions using two-level gate structures with a cost function depending on the own structure.

Enable students to design complex synchronous automata, including the use of partitioning techniques and hierarchical techniques, as well as simple asynchronous automata.

Knowing how to apply some of the methods used for encoding digital information for its transmission or storage in a compact or reliable way.

Knowing the methods used for verification and test to ensure the quality of digital electronic products.

Study load

<table>
<thead>
<tr>
<th>Total learning time: 112h 30m</th>
<th>Hours large group:</th>
<th>27h</th>
<th>24.00%</th>
</tr>
</thead>
<tbody>
<tr>
<td>Hours small group:</td>
<td>13h 30m</td>
<td></td>
<td>12.00%</td>
</tr>
<tr>
<td>Guided activities:</td>
<td>0h</td>
<td></td>
<td>0.00%</td>
</tr>
<tr>
<td>Self study:</td>
<td>72h</td>
<td></td>
<td>64.00%</td>
</tr>
</tbody>
</table>
# Content

<table>
<thead>
<tr>
<th>T1: Digital systems, logic gates and digital technologies (1.5 h)</th>
<th>Learning time: 3h</th>
</tr>
</thead>
</table>
Self study : 1h 30m |

<table>
<thead>
<tr>
<th>T2: Programmable logic devices as an alternative for the implementation of digital systems hardware (3 h)</th>
<th>Learning time: 6h</th>
</tr>
</thead>
</table>
| **Description:** Alternatives for the implementation of digital systems: hardware, software, and combination of hardware and software (co-design). Alternatives for the implementation of the digital systems hardware: off-the-shelf integrated circuits, full-custom integrated circuits, standard cells, gate arrays, and programmable logic devices. Cost analysis. Migrations. ASICs, ASSPs and SoCs. IP modules. Flexibility in logic and connections as the basis of programmable logic devices. Technologies and programmability of programmable logic devices. Precursors of actual programmable logic devices: ROMs, PLAs, PALs and sequential PALs. PLDs: macrocells. CPLDs. CPLD families: complexities. LCAs: configurable logic blocks. FPGAs: additional functional blocks (memory blocks, multipliers, DSP blocks, PLLs) and I/O standards selection. FPGA families. PSoCs: CPUs and digital and/or analog peripherals. PSoC families. The Cyclone III family from Altera. | Practical classes: 3h  
Self study : 3h |

<table>
<thead>
<tr>
<th>T3: Digital systems hardware design methodology (1.5 h)</th>
<th>Learning time: 3h</th>
</tr>
</thead>
</table>
Self study : 1h 30m |
| **T4: The VHDL hardware description language (6 h)** | **Learning time:** 12h  
Practical classes: 6h  
Self study : 6h |
| **Description:**  

| **T5: Extension of combinational systems (4.5 h)** | **Learning time:** 9h  
Practical classes: 4h 30m  
Self study : 4h 30m |
| **Description:**  

| **T6: Extension of sequential systems (6 h)** | **Learning time:** 12h  
Practical classes: 6h  
Self study : 6h |
| **Description:**  
## T7: Digital information encoding (6 h)

**Learning time:** 12h  
Practical classes: 6h  
Self study: 6h  

**Description:**  

## Laboratory experiments

**Learning time:** 26h  
Laboratory classes: 11h 30m  
Self study: 14h 30m  

**Description:**  
Experiment 1: Introduction to digital system hardware design based on programmable logic devices (3.5 h + 5.5 h)  
Experiment 2: Introduction to digital system hardware design using VHDL (2 h + 3 h)  
Experiment 3: Design of an automaton for the automatic opening and closing of a door using VHDL (2 h + 2 h)  
Experiment 4: Design of an automaton for reading a matrix keyboard using VHDL (2 h + 2 h)  
Experiment 5: Design of a control System with a secret key for the automatic opening and closing of a door using VHDL (2 h + 2 h)  

## Project

**Learning time:** 26h  
Laboratory classes: 0h 30m  
Self study: 25h 30m  

**Description:**  
VGA monitor controller for text display (0.5 h + 25.5 h)

## Assessment

**Learning time:** 3h 30m  
Practical classes: 3h 30m  

**Description:**  
Two partial exams.
The theory part will be assessed through two individual exams: a first partial exam at the beginning of the second half of the semester, and a second partial exam when ending the semester. The theory part will be globally re-assessed through an extraordinary unique exam, which will be held after the end of the ordinary exams period of the spring semester.

The laboratory part will be assessed through the development and documentation of the laboratory experiments and the project. The laboratory part will not be re-assessed after the end of the ordinary exams period of the spring semester. The last laboratory grades obtained in the semester or semesters allowing the re-assessment of the theory part will be used to calculate the grade appearing in the extraordinary academic record of students attending re-assessment.

The ordinary final course grade will be equal to the first of the following grades, rounded to the nearest tenth of a point, while the extraordinary final course grade will be equal to the following fourth possible final grade, rounded to the nearest tenth of a point:

\[
\begin{align*}
N_{\text{final1}} &= 0.25 N_{\text{pp1}} + 0.35 N_{\text{pp2}} + 0.20 N_{\text{lab}} + 0.20 N_{\text{proj}} \\
N_{\text{final2}} &= 0.60 N_{\text{extr}} + 0.20 N_{\text{lab}} + 0.20 N_{\text{proj}}
\end{align*}
\]

- $N_{\text{pp1}}$: Grade of first partial exam
- $N_{\text{pp2}}$: Grade of second partial exam
- $N_{\text{lab}}$: Grade of laboratory experiments
- $N_{\text{proj}}$: Grade of the project
- $N_{\text{extr}}$: Grade of extraordinary exam
- $N_{\text{final1}}$: Final grade (formula 1)
- $N_{\text{final2}}$: Final grade (formula 2)

?Not presented? will appear only in the academic record of students which have not attended any of the above-mentioned exams. The final course grade for those students that have attended at least one exam, but not all exams, will be calculated considering as zeroes the grades of the unattended exams. No grades will be kept on record for future semesters. No exams can be validated from the academic record of previous semesters.
Regulations for carrying out activities

The first partial exam of the theory part, which will consider chapters T1 to T4, will last an hour and a half. It will take place in one of the scheduled theory sessions of the course during the week immediately following the partial exams week.

The second partial exam of the theory part, which will consider chapters T5 to T7, will last for two hours. It will be held on the date and time set by Studies Planning for the final exam of the course.

Each one of the laboratory experiments should be shown and delivered to the professor, at most, two teaching weeks after the last laboratory session scheduled for this experiment. The project should be shown and delivered to the professor before two teaching weeks after finishing the course. Exam weeks will be considered as teaching weeks.

The extraordinary exam of the theory part, which will consider chapters T1 to T7, will last three hours. It will be held on the date and time set by Studies Planning for the extraordinary exam of the course.

The theory partial exams will consist in a set of short questions and problems.

Students may not bring any documentation, calculator, mass storage device information (floppy, CD, DVD, memory stick, etc.), nor communication device (cell phone, etc.) in any of the exams. Students must bring their identity card, passport or other official identification. Students violating these rules will be forced to leave the exam.

The grades of the exams will be published in the Digital Campus indicating the associated claim period.

Bibliography