240IEE21 - Design on Silicon

Coordinating unit: 240 - ETSEIB - Barcelona School of Industrial Engineering
Teaching unit: 710 - EEL - Department of Electronic Engineering
Academic year: 2019
Degree: MASTER'S DEGREE IN INDUSTRIAL ENGINEERING (Syllabus 2014). (Teaching unit Optional)
ECTS credits: 4,5
Teaching languages: Spanish

Teaching staff
Coordinator: LUZ M. BALADO SUAREZ
Others: Luz Balado Suárez
          Gómez Pau, Álvaro

Degree competences to which the subject contributes

Specific:
CEELECT1. Design electronic systems (mixed analogical and digital systems and micro-mechanical systems on silicon, digital systems based on discrete components, logical programable devices and/or microprocessors, electronic instrumentation systems and power electronic systems) and manage development projects and/or commercialization of electronic systems or development projects and/or commercialization of systems in which the electronic subsystems have an important specific weight.
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Teaching methodology

The course is structured in two parts: a theoretical part and a practical part. Each of these parts involves classroom activities, non-attendance activities and evaluation activities.

The course is assigned a load of 4.5 credits, which is equal to 112.5 hours of student dedication. 42 of these 112.5 hours will correspond to 26 hours of lectures and exercises, 10 hours of attendance to laboratory practices and 6 hours for assessments. The other 70.5 hours correspond to non-attendance activities (10h for circuit simulations and 60.5 hours of personal study and practice). The theoretical part includes theoretical presentations and resolution and/or discussion of problems and examples, going from one activity to another at the discretion of the teacher. The lectures will follow the program contents.

The theoretical activities will consist of lectures and problems solving, taking place during the weeks of the academic year, totaling a minimum of 26 classroom hours (13 sessions of 1 hour).

The practical part includes a project that will involve a set of circuits that must be simulated and/or assembled and experimented. The activities will consist of five laboratory practices in the schedules established for this purpose of duration of two hours, which will be developed in teams of two/three students. The number of students in the sessions of practice is limited to 15. Practices are held at the Electronics Laboratory II, located on the 9th floor. Each practice is associated with a set of tasks to be performed as a preparation for practice. It is also recommended carefully preparation prior practice, as significantly facilitates their understanding and their realization in the laboratory. The course is structured in two parts: a theoretical part and a practical part. Each of these parts involves classroom activities, non-attendance activities and evaluation activities.

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Learning objectives of the subject

It is a subject for specialists that has three main objectives:

1) CMOS process. The goal is to learn how integrate and manufacture an integrated circuit in CMOS technology. We study the technology of manufacturing CMOS nanometric processes and materials and techniques that are used in this process.

2) Layout level design. The objective is to present design techniques for analogue and digital layout. So OTA design and digital Full custom design are the main objectives.

3) Integration of mechanical devices in CMOS technology. Micro-machining techniques and their application in transducers are studied.
<table>
<thead>
<tr>
<th>Study load</th>
<th>Hours large group:</th>
<th>Total learning time: 112h 30m</th>
<th>Hours small group:</th>
<th>112h 30m</th>
<th>24.00%</th>
</tr>
</thead>
<tbody>
<tr>
<td>Total learning time: 112h 30m</td>
<td>27h</td>
<td>13h 30m</td>
<td>0h</td>
<td>0%</td>
<td>0.00%</td>
</tr>
<tr>
<td>Guided activities:</td>
<td>0h</td>
<td></td>
<td></td>
<td></td>
<td>0.00%</td>
</tr>
<tr>
<td>Self study:</td>
<td>72h</td>
<td></td>
<td></td>
<td></td>
<td>64.00%</td>
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<table>
<thead>
<tr>
<th>Content</th>
<th>Learning time:</th>
<th>Description:</th>
<th>Related activities:</th>
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</thead>
</table>
Self study: 1h |
| **T2. CMOS Technology** | 21h | Alternatives to silicon manufacturing. MOS transistor. MOS transistor layout. MOS capacitances. MOS transistor technologies. CMOS technologies. CMOS inverter. Static characteristics. Dynamic characteristics. Dynamic behaviour. | Theory classes: 5h  
Laboratory classes: 2h  
Self study: 14h |
Laboratory classes: 2h  
Self study: 7h |

**Related activities:**
- P1. Layout design tool (Microwin) - Ring oscillator
- P5. Complete design of a mixed-signal circuit
<table>
<thead>
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<th>Description</th>
<th>Learning time</th>
<th>Related activities</th>
</tr>
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</table>
The theoretical part will be assessed through two tests of individual character: a partial test first half of the semester, a final exam when the course has ended.

The practical part will be evaluated by three notes. The grade evaluation of the project presented the note of continued evaluation and the note for individual development of the student in the group.

The rating actions will follow the equation below, rounded to the nearest tenth of a point:

\[ N_{\text{final1}} = 0.20 \times N_{\text{pp}} + 0.4 \times N_{\text{pf}} + 0.2 \times N_{\text{ap}} + 0.10 \times N_{\text{ac}} + 0.10 \times N_{\text{ai}} \]

- \( N_{\text{pp}} \): partial test
- \( N_{\text{pf}} \): final test
- \( N_{\text{ap}} \): Project evaluation
- \( N_{\text{ac}} \): Continuous evaluation
- \( N_{\text{ai}} \): Individual evaluation

The reassessment process of the subject in July will be done on the theoretical test with the same characteristics as the final exam. The new note replaces obtained in June in the expression of the final grade.

Due to covid19, the evaluation of 2019-2020 Q2 will follow the equation: \( N_{\text{final}} = 0.4N_{\text{pf}} + 0.3N_{\text{ap}} + 0.2N_{\text{ac}} + 0.1N_{\text{ai}} \)

### Qualification system

<table>
<thead>
<tr>
<th>T7. Silicon MEMs</th>
<th>Learning time: 9h</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Theory classes: 3h</td>
</tr>
<tr>
<td></td>
<td>Self study: 6h</td>
</tr>
</tbody>
</table>

**Description:**

<table>
<thead>
<tr>
<th>T8. Case study of an integrated sensor</th>
<th>Learning time: 3h</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Theory classes: 1h</td>
</tr>
<tr>
<td></td>
<td>Self study: 2h</td>
</tr>
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</table>

**Description:**

<table>
<thead>
<tr>
<th>T9. Beyond CMOS</th>
<th>Learning time: 4h 30m</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Theory classes: 1h 30m</td>
</tr>
<tr>
<td></td>
<td>Self study: 3h</td>
</tr>
</tbody>
</table>

**Description:**
Regulations for carrying out activities

The first part of the theory test will last two hours and will consist of a series of questions and designs related to the lecturers until the day of the test. The test will last 3 hours and will consist of a series of questions and designs the entire syllabus of the subject.

Students must carry their ID card, passport or other official identification document.

The scores of the tests will published in the Digital Campus. Regarding the qualifications of laboratory will be published during the week following the completion of the course, opening a period of claims ending the day before the final test of the theory.

Bibliography

Basic: